METHOD FOR FABRICATING MOS TRANSISTORS

BACKGROUND OF THE INVENTION

Field of the invention

The present invention relates to a method for fabricating semiconductor devices, more particularly to a method for fabricating metal oxide semiconductor (MOS) transistors, which can reduce the junction capacitance without a degradation of characteristics in a transistor even in gate line narrowing.

Description of the Prior Art

As generally known in the art, with the high-integration of semiconductor devices, the line narrowing of a gate electrode has been caused so that the length of a channel has been reduced, which generates a short channel effect by which threshold voltage of a transistor is rapidly reduced. Thus, various technologies have been proposed so as to reduce the short channel effect.

Herein, the prevention of the short channel effect is a problem to be solved for a high integration of a semiconductor device. One way to solve the problem is to form a lightly doped drain (LDD) region.

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An MOS transistor of the prior art adapting LDD structure will be now described with reference to FIGS. 1A to 1C.

Referring to FIG. 1A, ion implantation processes for well formation, field stop formation, punch stop formation and threshold voltage adjustment are successively conducted to the whole area of a semiconductor substrate 1 having a trench type isolation layer 2. Then, a gate oxide layer 3a and a gate conductive layer 3b are successively formed, and the gate oxide layer 3a and the gate conductive layer 3b are patterned to form a gate electrode 4.

Referring to FIG. 1B, ion implantation of low concentration impurities is conducted to the semiconductor substrate 1 including the gate electrode 4 to form LDD regions 5 on both side portions of the gate electrode 4. Then, an oxide layer 6a and a nitride layer 6b are successively deposited on the semiconductor substrate 1 so as to cover the gate electrode 4.

Referring to FIG. 1C, the oxide layer 6a and the nitride layer 6b are blanket etched to form spacers 7 on both side walls of the gate electrode 4. Then, ion implantation of high concentration impurities is conducted to the whole area of the substrate, and an annealing treatment is conducted to former to form source/drain regions 8 with an LDD region 5 formed in the

substrate on both side portions of the gate electrode 4.

However, in the fabricating method of MOS transistor of the prior art, ion implantation processes for well formation, field stop formation, punch stop formation and threshold voltage adjustment are successively conducted to the whole area of active region of the semiconductor substrate so as to reduce a shot channel effect, thus increasing dopants concentration of well in the source/drain regions.

In this case, the increase of the dopants concentration of well causes a generation of the junction capacitance in the source/drain region, and the junction capacitance causes a delay of gate signal, which functions to reduce reliability of the semiconductor device. Particularly, these are one of the problems to be solved in conjunction with the tendency of gradual increase of degradation of device characteristics due to a short channel effect according to a gradual reduction of critical dimensions of the gate electrode.

SUMMARY OF THE INVENTION

Accordingly, the present invention has been made to solve the above-mentioned problems occurring in the prior art, and an object of the present invention is to provide a method for

fabricating MOS transistors, which can reduce the junction capacitance without a degradation of characteristics in a transistor even in gate line narrowing.

In order to accomplish this object, there is provided a method for fabricating MOS transistors, the method comprising the steps of: forming a buffer oxide layer on a semiconductor substrate having an isolation layer; successively conducting ion implantations for well formation and field stop formation in an active region of the substrate through the buffer oxide layer; removing the buffer oxide layer; forming a sacrificial layer of the semiconductor substrate; patterning the sacrificial layer to form a trench defining a gate electrode forming region; successively conducting ion implantations for threshold voltage adjustment and punch stop formation on the semiconductor substrate area exposed by the trench; forming a gate oxide layer on the surface of the substrate under the bottom face of the trench; forming a polysilicon layer on the sacrificial layer so as to completely bury the trench; polishing the polysilicon layer until the surface of the sacrificial layer is exposed, so as to form a gate electrode; removing the sacrificial layer; forming an LDD region in the surface of the substrate at both side portions of the gate electrode; forming spacers on both side walls of the gate

electrode; and forming the source/drain regions in the surface of the substrate at both side portions of the gate electrode including the spacers.

According to the present invention, since the ion implantations for threshold voltage adjustment and punch stop formation are conducted only to the channel region, an increase of the junction capacitance can be prevented, thus avoiding degradation of characteristics of devices.

BRIEF DESCRIPTION OF THE DRAWINGS

The above and other objects, features and advantages of the present invention will be more apparent from the following detailed description taken in conjunction with the accompanying drawings, in which:

FIGS. 1A to 1C are end views showing a fabricating method of MOS transistors of the prior art according to every processes; and

FIGS. 2A to 2E are end views showing a fabricating method of MOS transistors of an embodiment of the present invention according to every processes.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Hereinafter, a preferred embodiment of the present invention will be described with reference to the accompanying drawings. In the following description and drawings, the same reference numerals are used to designate the same or similar components, and so repetition of the description of the same or similar components will be omitted.

FIGS. 2A to 2E are end views showing a fabricating method of MOS transistors of an embodiment of the present invention according to every processes.

Referring to the FIG. 2A, a buffer oxide layer 25 is formed on a semiconductor substrate 21 having a trench type isolation layer 23. Then, ion implantations for well formation and field stop formation are successively conducted to an active region of the substrate 21 through the buffer oxide layer 25.

Referring to the FIG. 2B, the buffer oxide layer is removed and a sacrificial layer 27 composed of a chemical vapor deposition (CVD) oxide layer is formed on the semiconductor substrate 21 so as to have a thickness ranging for example between 500□ and 1000□, corresponding desired thickness of a gate electrode. Then, the sacrificial layer 27 is patterned to

form a trench 29 defining a gate electrode forming region according a conventional photolithography process. In this case, the patterning of the sacrificial layer is implemented by wet-etching process. Then, ion implantations for threshold voltage adjustment and punch stop formation are successively implemented only on an area of the semiconductor substrate 21, i.e., a channel formation region of MOS transistor. As a result, ion implantation for field stop formation is conducted only under the to-be-gate electrode area. The impurity for well formation and field stop formation is boron or phosphorous or Arsenic. Implant is made at a sufficient energy to form specific region, for example, barriers below the source /drain junction for well and field stop or threshold voltage adjustment and punch stop.

Referring to the FIG. 2C, a gate oxide layer 31a is formed on the surface of the substrate 21 under the bottom face of the trench 29 using an oxidation process, and a polysilicon layer 31b is formed on the sacrificial layer 27 so as to completely bury the trench 29.

Referring to the FIG. 2D, the polysilicon layer 31b is polished until the surface of the sacrificial layer is exposed, thus forming a gate electrode 31. Then, after the sacrificial

layer is removed, an LDD region 33 is formed by an ion implantation of low concentration impurities and a subsequent annealing treatment for the resultant substrate.

Referring to the FIG. 2E, an oxide layer 37a and a nitride layer 37b are successively formed on the whole area of the substrate so as to cover the gate electrode 31. Then, the oxide layer 37a and the nitride layer 37b are blanket etched to form spacers 37 on both sidewalls of the gate electrode 37. Then, the source/drain regions 35 are formed in the surface of the substrate at both side portions of the gate electrode 37 by an ion implantation of high concentration impurities and a subsequent annealing treatment for the substrate resulted from the previous step. With the result of the former steps, MOS transistor of the present invention is achieved.

According to the present invention, since the ion implantations for threshold voltage adjustment and punch stop formation are conducted only to the channel forming region, an increase of the junction capacitance can be prevented in comparison with the conventional technology in which all fabricating procedures thereof are conducted to the whole area of the active region.

As described above, in the fabricating method of MOS transistor of the present invention, a trench defining a gate

electrode region is formed, and ion implantation processes for threshold voltage adjustment and punch stop formation are conducted only to the channel forming region using the trench, thus preventing an increase of dopants concentration of well in the source/drain regions. Accordingly, the junction capacitance can be reduced without a degradation of the characteristics of the transistor even though a length of the gate electrode is reduced, reducing a delay of gate signal and thus improving reliability of semiconductor devices.

Although preferred embodiments of the present invention have been described for illustrative purposes, those skilled in the art will appreciate that various modifications, additions and substitutions are possible, without departing from the scope and spirit of the invention as disclosed in the accompanying claims.